422 - Hardware & Organization

Progress Report #2

**Smart Cafe**

Helina Azer

Daniella Pairault

Alex Petrenko

Eric Pham

## What We Accomplished:

* I/O routines written; other APIs documented in code
* Partial test file written and taken into main source file and tested
* Input test file successfully taken in and output file successfully written and pushed.

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| **Instructions:** | | **Addressing Modes:** |
| 1. NOP 2. MOVE 3. MOVEM 4. ADD 5. SUB 6. MULS 7. DIVU 8. LEA 9. AND 10. NOT 11. LSL | 1. LSR 2. ASL 3. ASR 4. BLT 5. BGE 6. BEQ 7. JSR 8. RTS 9. BRA | 1. Data Register Direct 2. Address Register Direct 3. Address Register Indirect 4. Immediate Addressing 5. Address Register Indirect with Post Incrementing 6. Address Register Indirect with Pre Decrementing 7. Absolute Long Address 8. Absolute Word Address |

## Problems Encountered:

* We are a bit stuck on how to start disassembling opcodes and addressing modes
  + We will need guidance from Professor Hogg on where to start (private office hours)

## Are We on Track?

* We were hoping to have some of the opcodes and addressing modes done for progress report 2, but we couldn’t get to it. We will work extra hard the next two weeks to have the majority if not all of the opcodes and addressing modes done for progress report 3.

## Next Progress Report:

* Scan the test file (Test.X68) and write out the raw hex (Progress Report #3)
* Disassemble simple instructions: NOP, JSR, etc (Progress report #3)
* Disassemble more instructions (Progress report #3)
* Handle addressing modes (Progress report #3)

## Future Progress Reports:

1. Error handling (Progress report #4)
2. Remaining instructions & addressing modes (eg: MOVEM) (Progress report #4)
3. Check against Test (Progress report #4)
4. Gather final report (Progress report #4)